EE/CE 3310 - "Intel, Synopsys, TSMC All Unveil Record Memory Densities" Alex Kader

In the article "Intel, Synopsys, TSMC All Unveil Record Memory Densities," Samuel K. Moore discusses the growing gap between logic and memory scaling in modern semiconductor manufacturing [1]. While transistor density for logic has continued to improve, static random-access memory (SRAM) has hit a "scaling wall" due to leakage and imperfect process variations [1]. To help solve this issue, two of the largest advanced chipmakers — Intel and TSMC — are transitioning to nanosheet transistor architectures, also known as gate-all-around (GAA) FETs. At the ISSCC last year, both companies demonstrated record SRAM densities of approximately 38.1 Mb/mm^2 using their respective 18A and N2 architecture technologies [1]. Another manufacturer, Synopsys, showed that similar densities could be achieved on older 3nm nodes, albeit at lower operating frequencies. This move to GAA nanosheets enables better electrostatic control of the transistor channels, allowing operating voltages down to 0.6V, which is critical for the energy and efficiency demands of AI hardware [1].

To better understand the physics behind the switch, I found two articles discussing the structural and circuit-level implications of nanosheet FETs. According to N. Loubet et al., the transition to stacked nanosheets is essential for maintaining gate control as gate lengths continue to shrink [2]. Their research shows that by vertically stacking silicon channels, manufacturers can increase the effective channel width within a smaller footprint, which keeps the required drive current and reduces off-state leakage [2]. In addition, P. Weckx et al. highlight how this GAA control specifically benefits memory arrays by introducing a "fork" architecture to save space [3]. They explain that the reduced variability and improved subthreshold swing in nanosheet-based devices significantly improve the noise margin of SRAM cells. This new stability enables the bit cells to operate reliably at the extremely low voltages mentioned in Moore's article [1], directly addressing the challenges of keeping up with the rapid scaling of transistors [3].

[1] S. K. Moore, "Intel, Synopsys, TSMC All Unveil Record Memory Densities," *IEEE Spectrum*, Feb. 26, 2025. [Online]. Available: https://spectrum.ieee.org/sram-intel-tsmc. [Accessed 18 April, 2026].

[2] N. Loubet *et al*., "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET," *2017 Symposium on VLSI Technology*, Kyoto, Japan, 2017, pp. T230-T231, doi: 10.23919/VLSIT.2017.7998183.

[3] P. Weckx *et al*., "Stacked nanosheet fork architecture for SRAM design and device co-optimization toward 3nm," *2017 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2017, pp. 20.5.1-20.5.4, doi: 10.1109/IEDM.2017.8268430.